VII-046

Roll No. [redacted] Total Printed Pages : 5

07BEC105

B.TECH (ELECTRONIC & COMM. ENGG.)

VII SEM Examination, Dec.-2017

SUB : VLSI DESIGN

Time : 3 Hours] [Total Marks 60

Use of following supporting material is permitted during examination.

1. Nil _____ . _____ Nil

Note: 1. Attempt any five questions selecting one question from each unit.

2. Each question carry equal marks.

UNIT-I

1. a. Describe the SSI, MSI, LSI, VLSI and ULSI on the basis of number of components in an IC and also define moore law.

b. Draw the transfer conductance characteristics of:

i. NMOS Deplition mode MOSFET

ii. PMOS enhancement mode MOSFET

OR

2. a. Explain P-well process in CMOS fabrication with suitable diagram?

b. Derive an expression bar pull up and pull down ratio of NMOS Inverter driven by a NMOS inverter.

UNIT-II

3. a. Explain the basic step for fabrication of CMOS N-well process?

b. Prove equation for V-I relationship of MOS transistor?

OR

4. a. Explain operation of enhancement NMOS MOSFET?

b. Draw the I_D-V_{DS} characteristics of following type of MOSFET

i. n-channel depletion type of MOSFET

ii. n-channel enhancement type MOSFET

iii. p-channel depletion type MOSFET

iv. p-channel Enhancement type MOSFET

UNIT-III

5. Implement following circuit using CMOS (any two)

a. 2x1 MUX

b. D-flip flop

c. $A + BC + \overline{CD}$

d. $\overline{\bar{A}\bar{B}\bar{C} + \bar{A}BC + \bar{A}B\bar{C} + ABC}$

e. $A\,B\,C + \bar{A}\,\bar{B}\,C$

OR

6. Find the equivalent (W/L) ratio of NMOS and PMOS transistor in the given circuit.